

1/17

Fig. 1

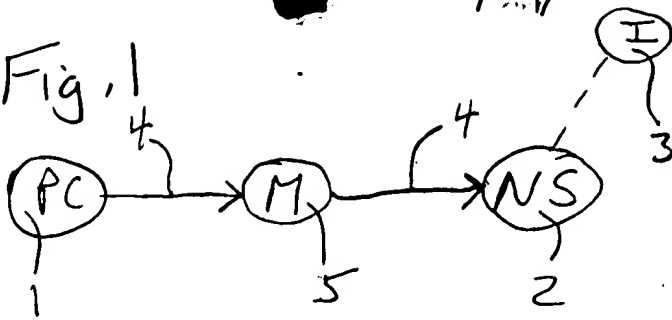


Fig. 2

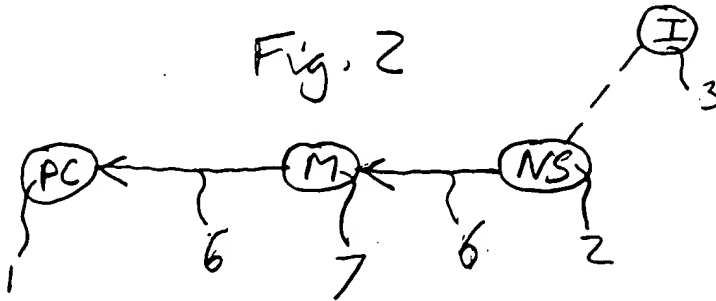


Fig. 3

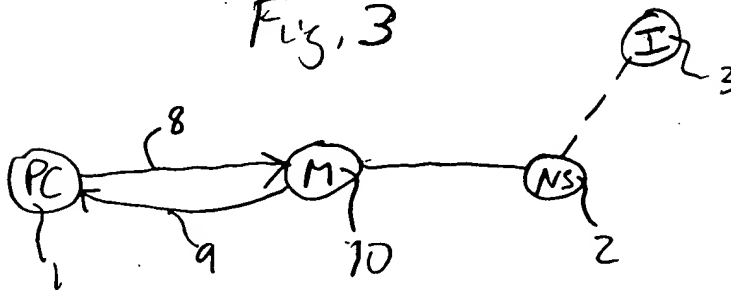


Fig. 4A

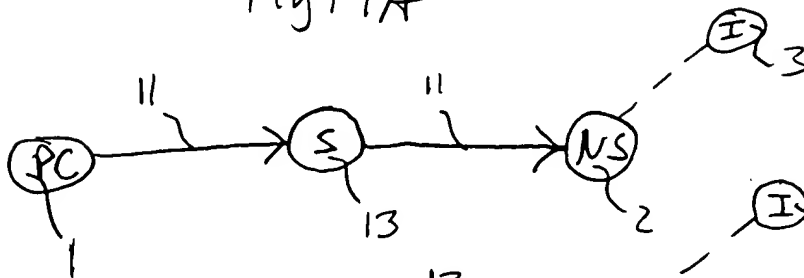


Fig. 4B

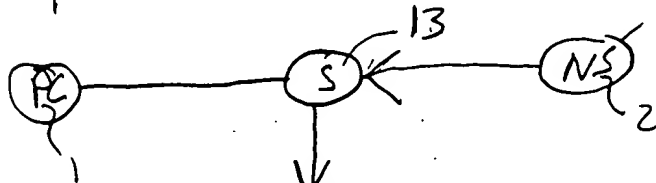
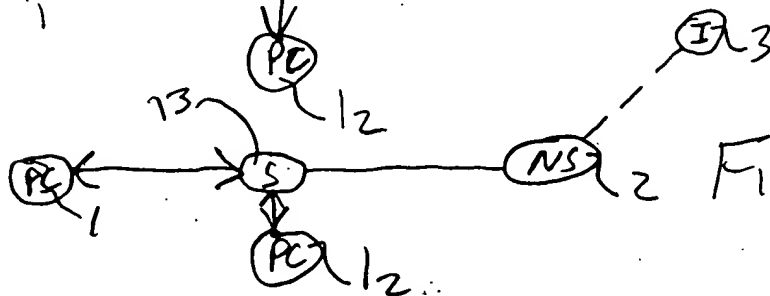


Fig. 4C



2/17

Fig. 5A

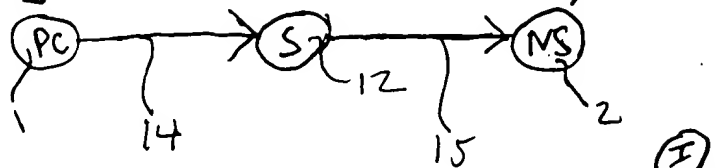


Fig. 5B

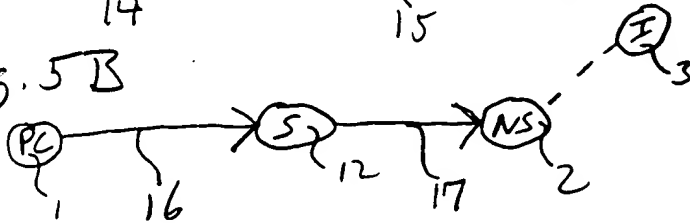


Fig. 6

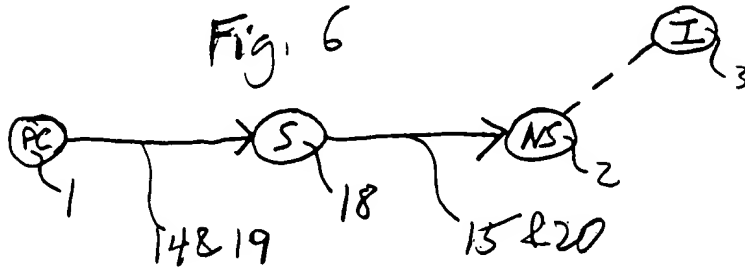


Fig. 7

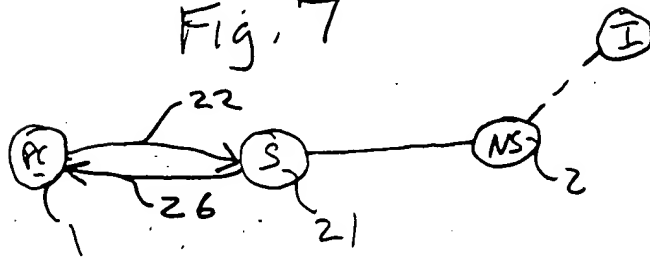
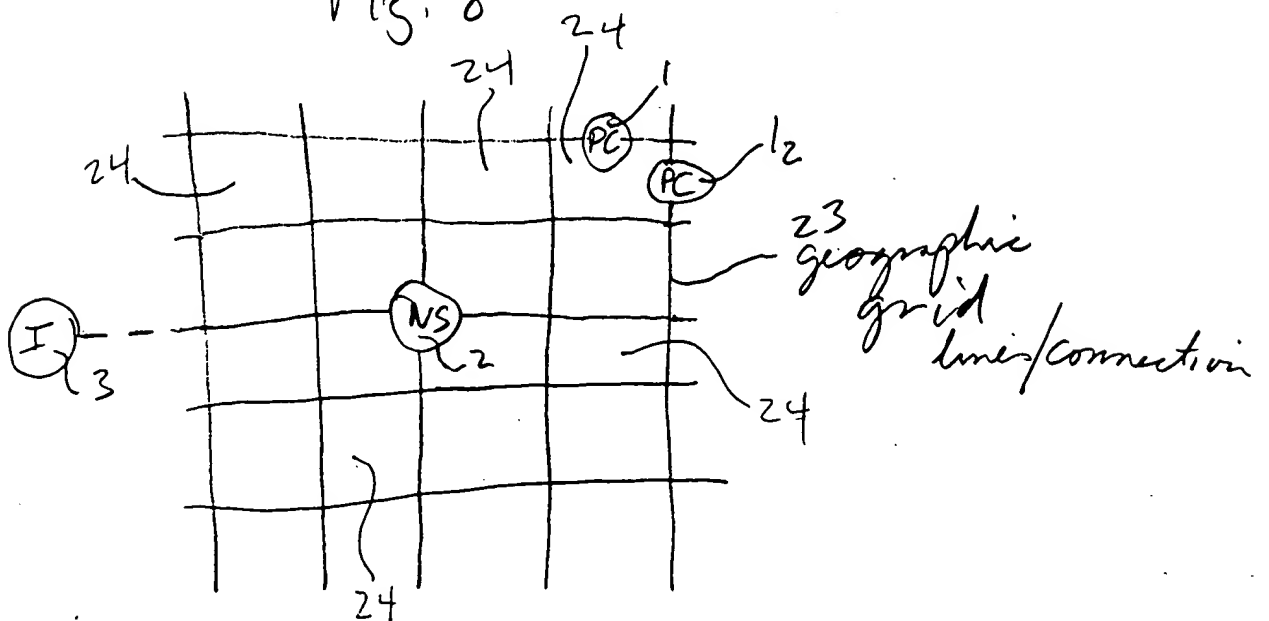


Fig. 8



30

M

50

40

✓ 1 PC

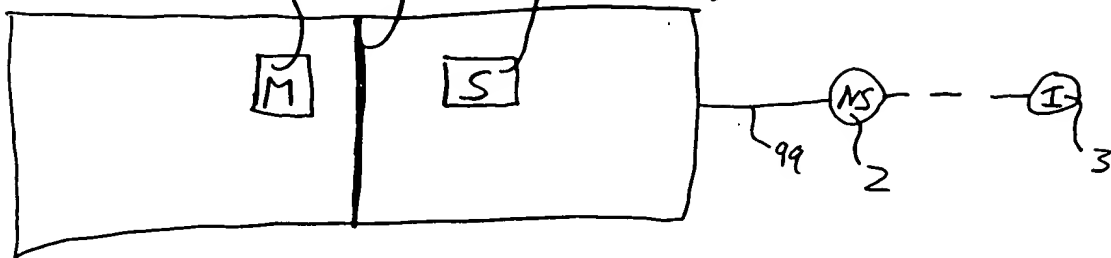
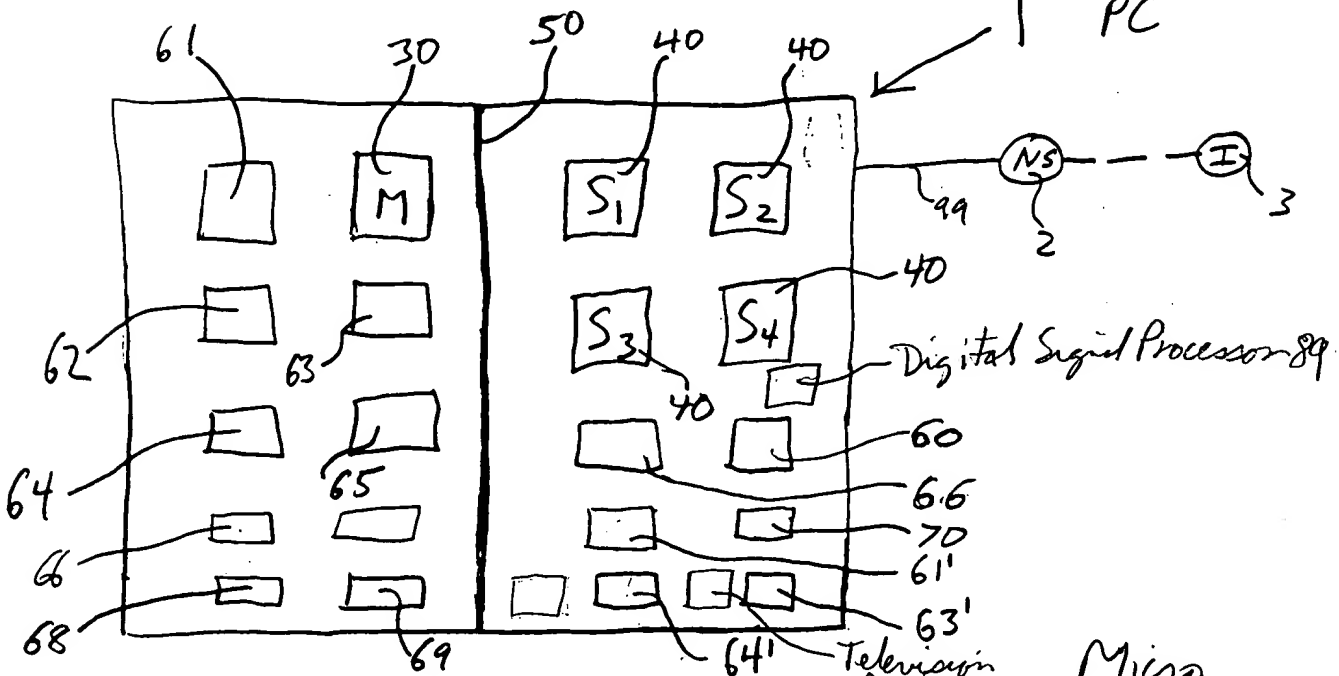


Fig. 10A

1 PC



Television  
Review

Micro  
Chip  
(PC on  
a chip)

Fig. 10 C

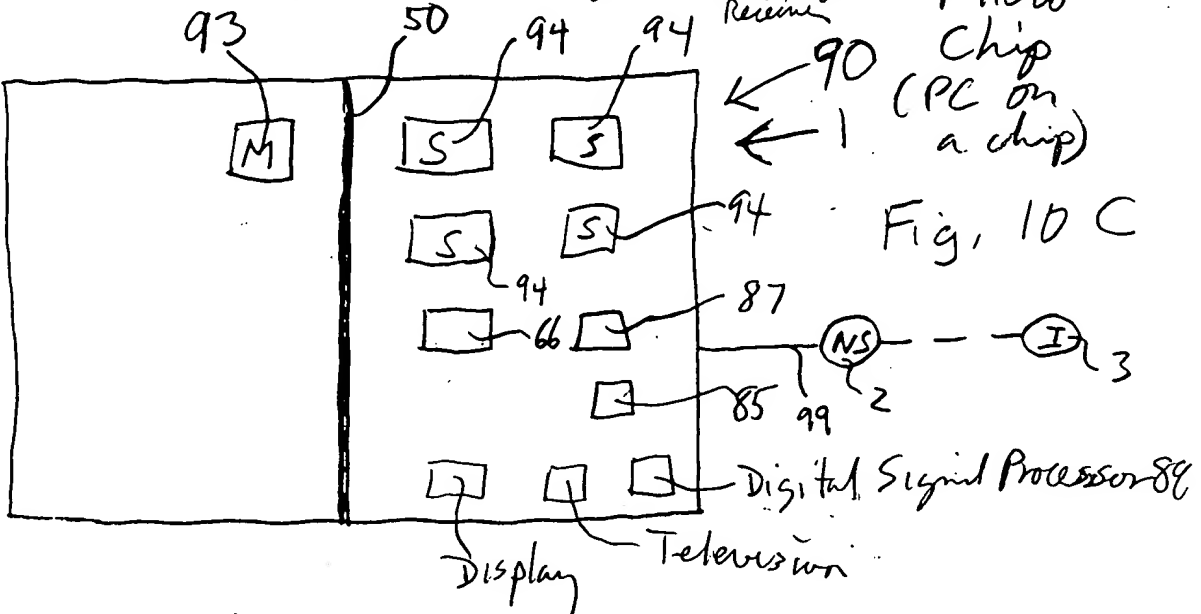


Fig. 9

4/17

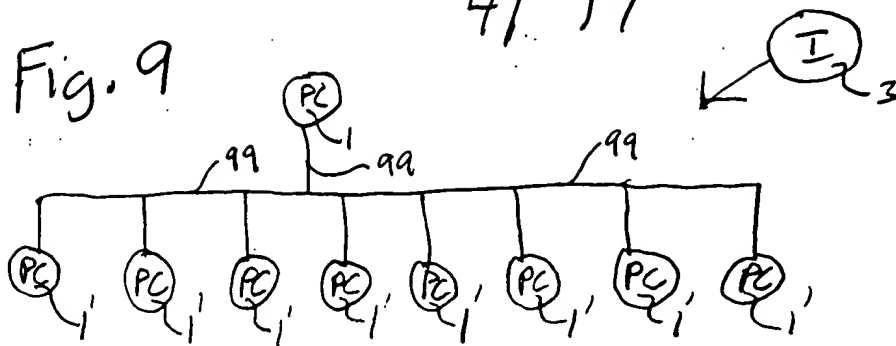


Fig. 10 D

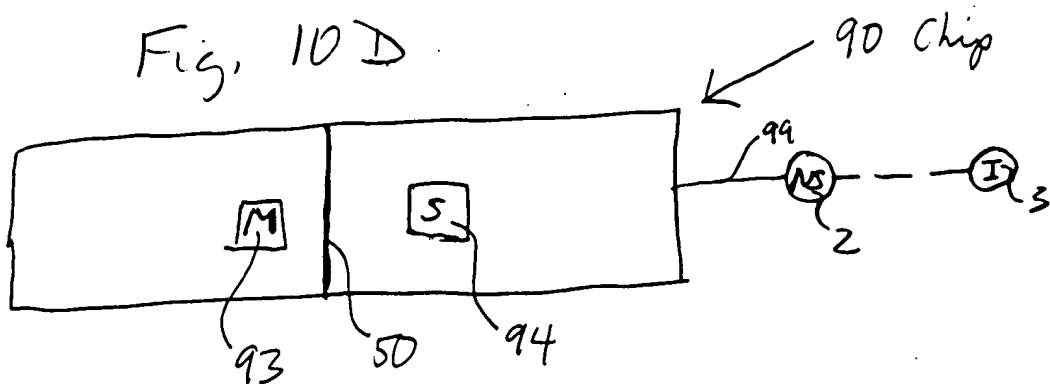


Fig. 11

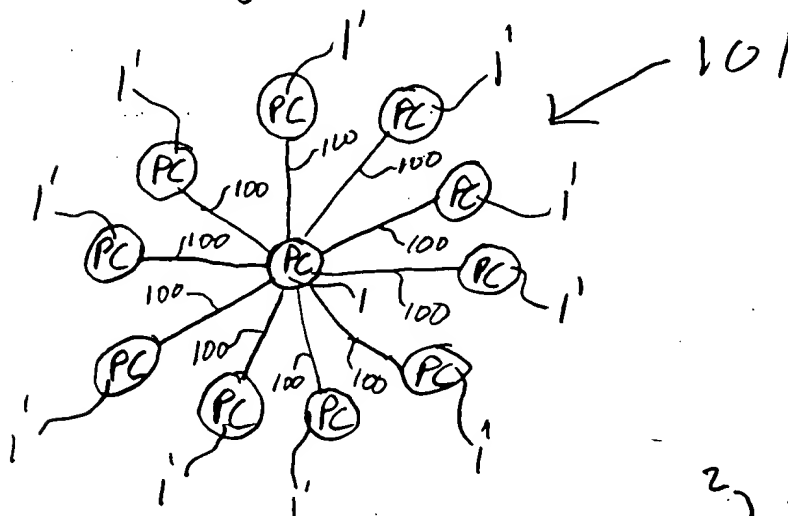
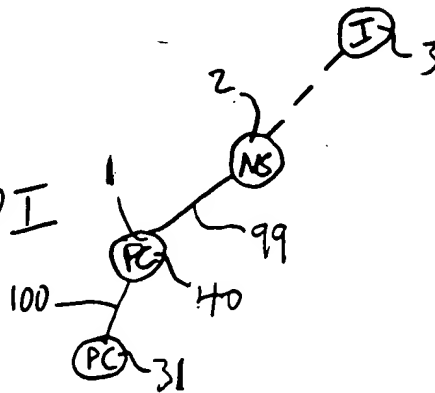


Fig. 10 I



2025 RELEASE UNDER E.O. 14176

5/17

Fig. 10E

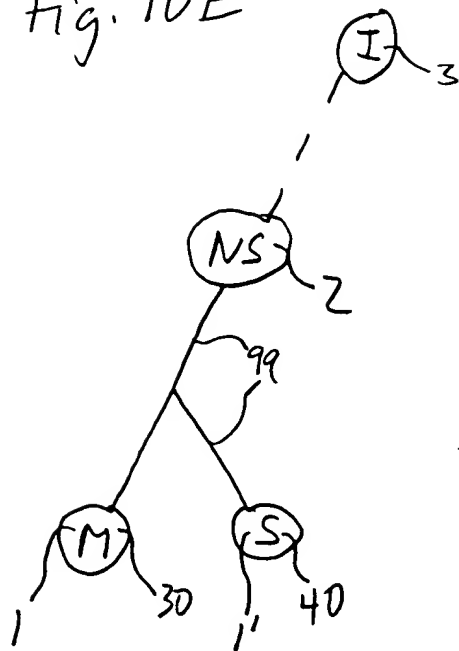


Fig. 10F

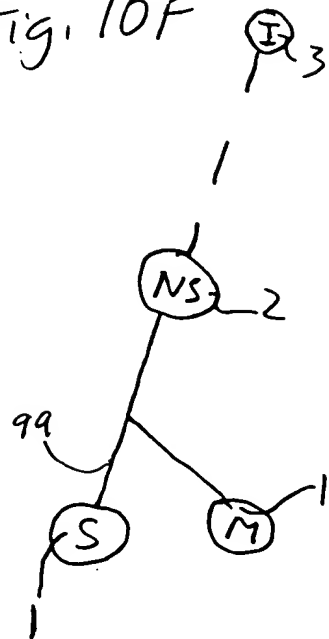


Fig. 10G

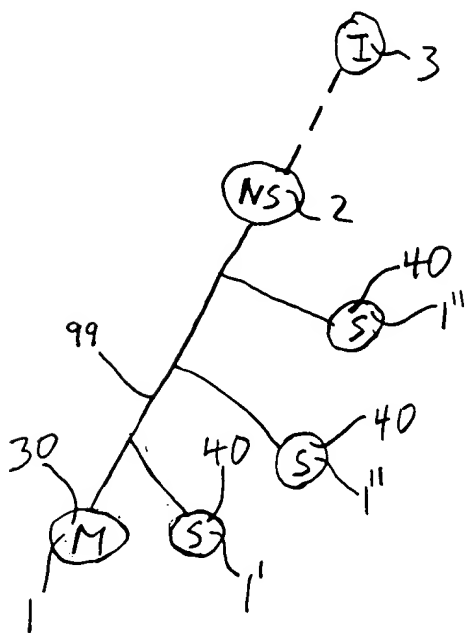


Fig. 10H

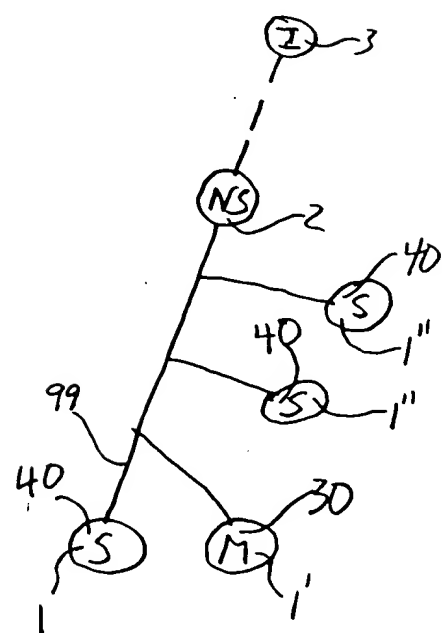


Fig. 12

```
graph TD; Root(( )) --- 100[100]; Root --- 110[110]; 100 --- PG1((PG1)); 110 --- I3((I3))
```

Fig. 14A

The diagram illustrates a network topology. A central node, labeled 120, is connected to five peripheral nodes, each also labeled 120. The nodes are represented by circles containing the letters 'PC'. The connections are labeled with reference numerals 105 and 106. A reference numeral 101 points to the diagram.

7/17

Fig. 10K

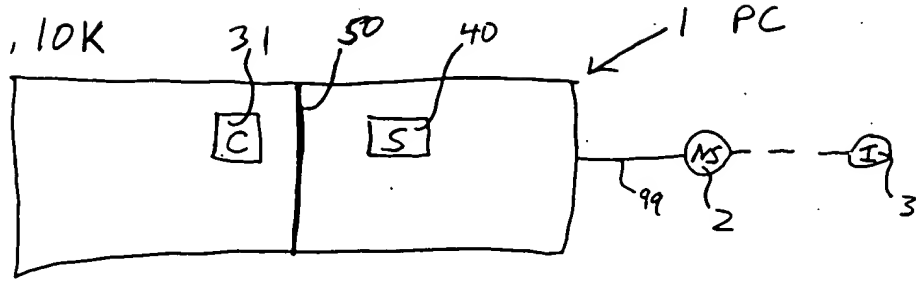


Fig. 10J

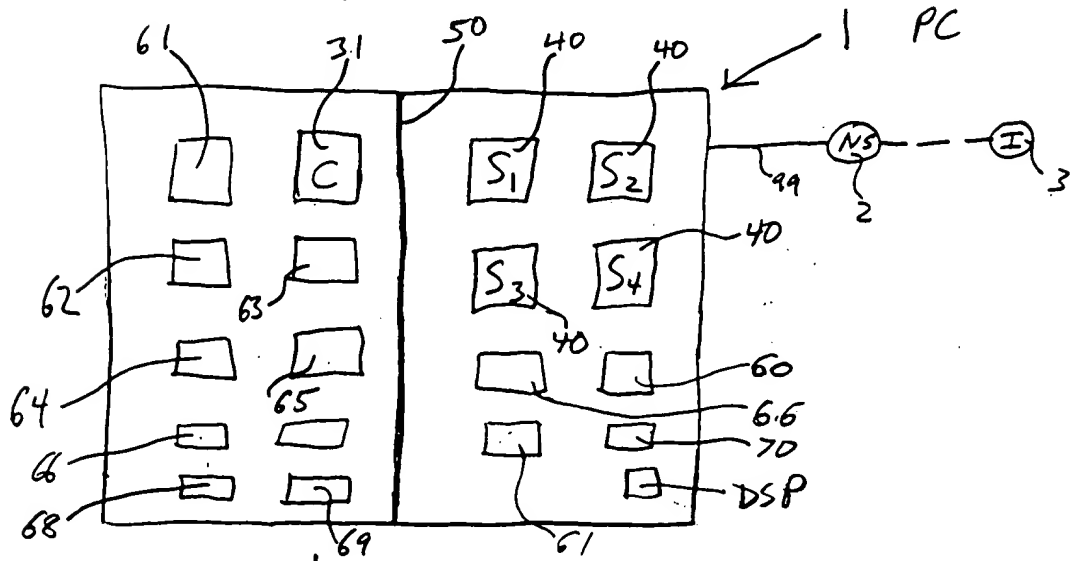


Fig. 10L

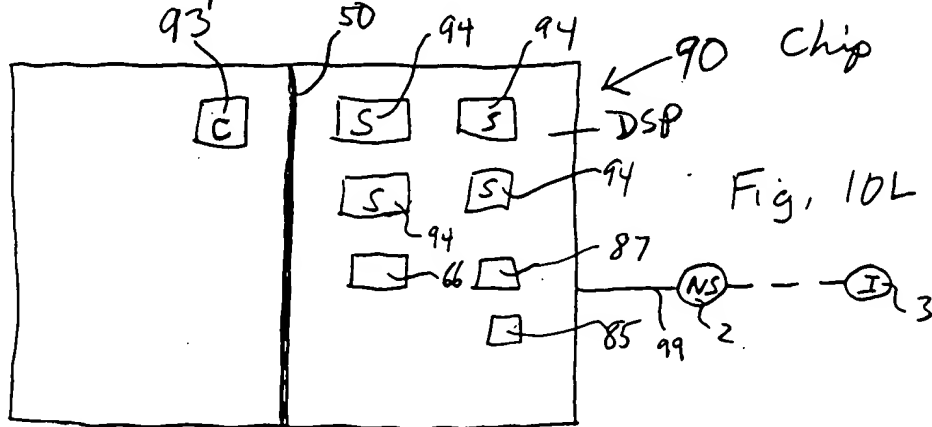
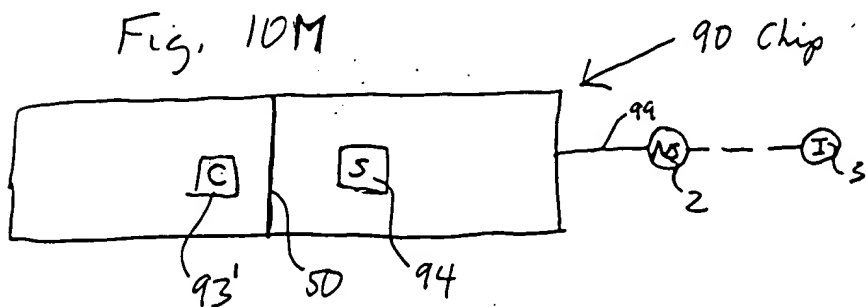


Fig. 10M



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Fig. 10"0"

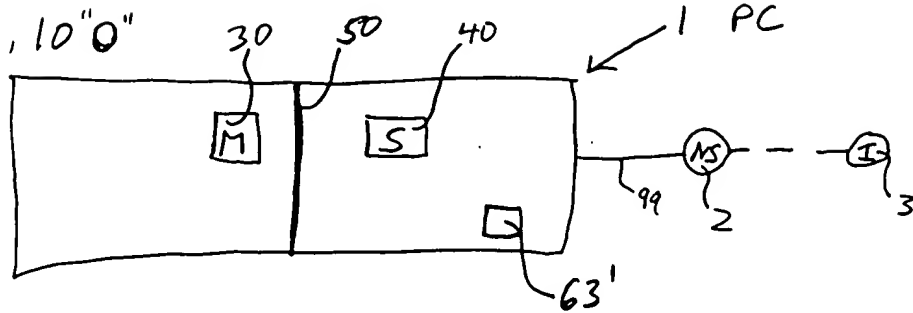
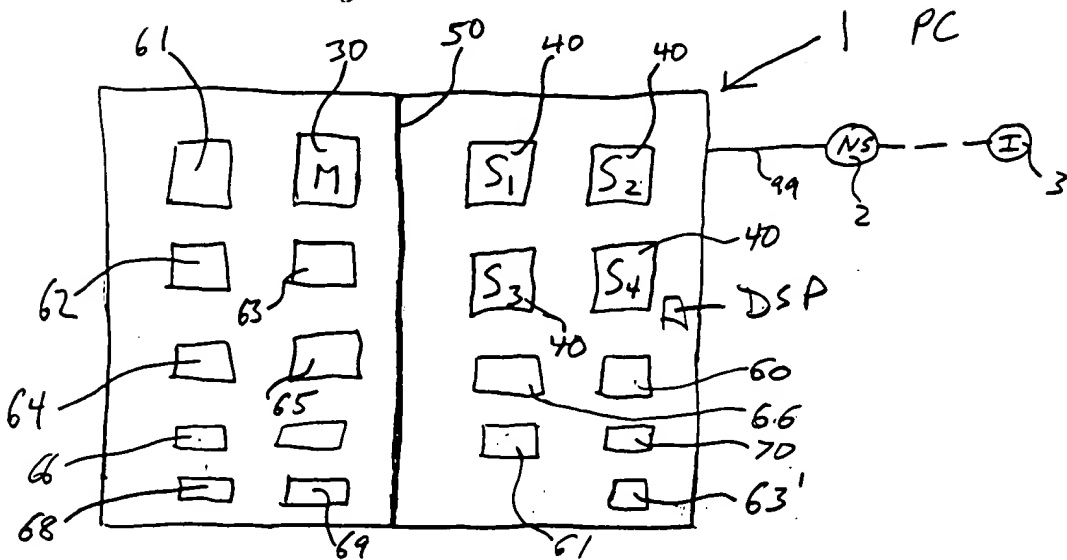


Fig. 10N



93

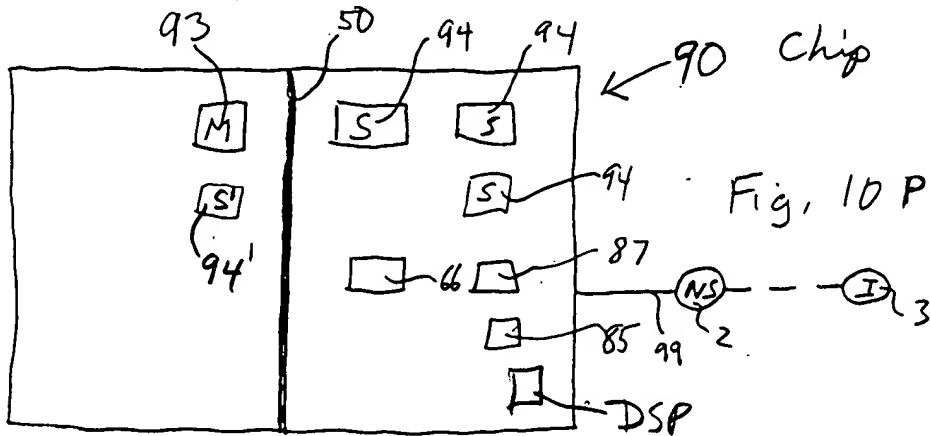
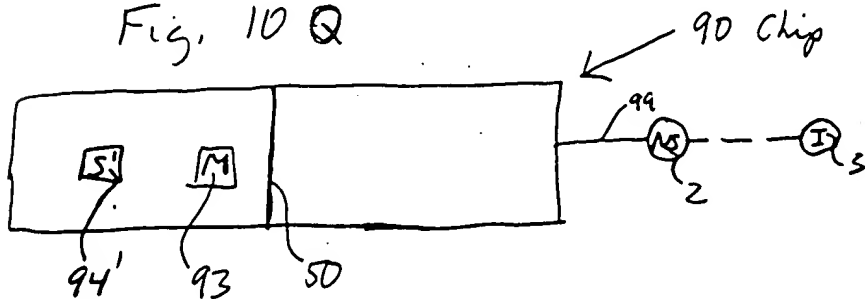


Fig. 10 Q





[illegible]

Diagram illustrating a three-port network configuration. The central node is labeled  $M_1$  (value 30). The two side nodes are labeled  $S_{21}$  (value 40) and  $S_{22}$  (value 40). The connections between the nodes are labeled with values: 99 for the connection between  $M_1$  and  $S_{21}$ , and 99 for the connection between  $M_1$  and  $S_{22}$ . The horizontal line connecting  $S_{21}$  and  $S_{22}$  is labeled with 99. The text "optical fiber on wire" is written below the horizontal line.

← (I) (Part of Internet or Intranet or other net)  
3  
wire

A hand-drawn diagram of a person with an arrow pointing left, labeled '3'.

Figs 16A-Q &  
16V-AA?

③① indicates either master PC 1 or master microprocessor 30 chips within a PC1.

Like vice, 1-40 indicates either a slave PCI or a slave microprocessor 40 chip within a PCI.

A diagram of a three-bus system. The buses are represented by circles containing their voltage magnitudes: the left bus is labeled  $S_{21}$  and contains the value 40; the middle bus is labeled  $M_1$  and contains the value 30; the right bus is labeled  $S_{22}$  and contains the value 40. The buses are connected by a horizontal line representing a transmission line. A fault, indicated by a cross on the line and labeled 'gg' below it, is located on the segment between the middle bus  $M_1$  and the right bus  $S_{22}$ . Each bus has a small '1' above it, possibly indicating a phase or a specific point of interest.

Either microprocessor  
300 microprocessor  
40 can be a  
microprocessor 90,  
a PCI or a microcontroller

99

1 wireless 1

100

$S_1$  (40)  $M_1$  (30)

Note 100: mix of 100g 94

③

operation to  
Slave PC?  
what functions is it

I

Diagram I shows a network with four nodes, each labeled with a superscript 1 and a subscript:  $S_{21}^1$ ,  $S_{21'}^1$ ,  $S_{31}^1$ , and  $S_{32}^1$ . Each node contains the number 40. The nodes are arranged in a square pattern.  $S_{21}^1$  and  $S_{21'}^1$  are at the top, connected by a horizontal line with '99' above it.  $S_{31}^1$  and  $S_{32}^1$  are at the bottom, connected by a horizontal line with '99' below it. A vertical line connects  $S_{21}^1$  and  $S_{31}^1$ , and another vertical line connects  $S_{21'}^1$  and  $S_{32}^1$ . Both vertical lines have a diagonal slash through them.

A hand-drawn diagram of a node. It consists of a circle containing the letter 'I'. A horizontal arrow points to the left from the circle. A wavy line extends downwards from the bottom of the circle, with the number '3' written at its end.

Unavailable  
S21 off/loads  
results of S31 & S32  
to S21, which takes  
available over

Diagram of a three-bus power system. Bus 1 (30 MW) is connected to Bus 2 (40 MW) and Bus 3 (I MW). Bus 2 is also connected to Bus 3. The diagram shows a central bus connected to three other buses, with power flows indicated by arrows and labels like  $S_{21}$ ,  $S_{22}$ , and  $S_3$ .

Like Fig. 16 D  
 $S_{21}'$  replaces  $S_{21}$

10/17

Fig. 16 E

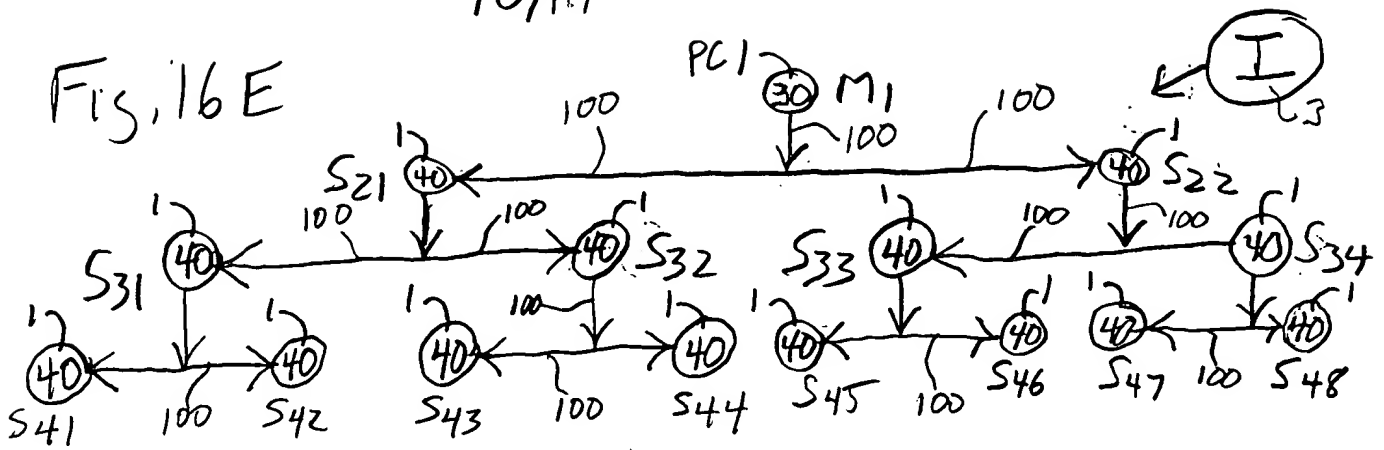


Fig. 16 F

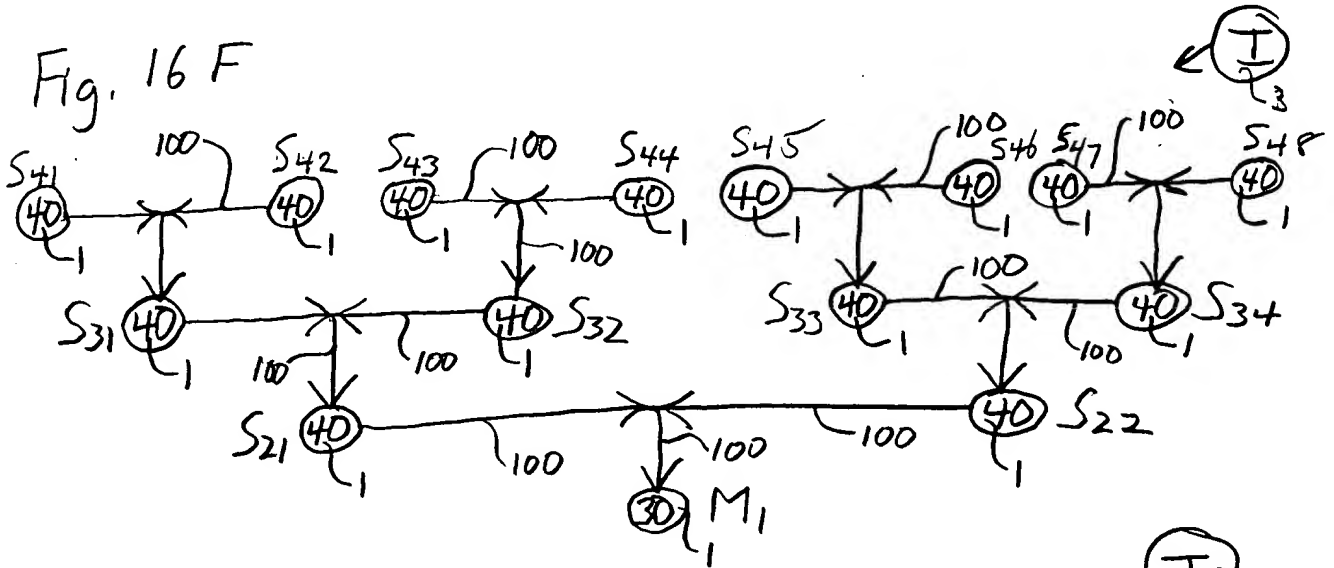
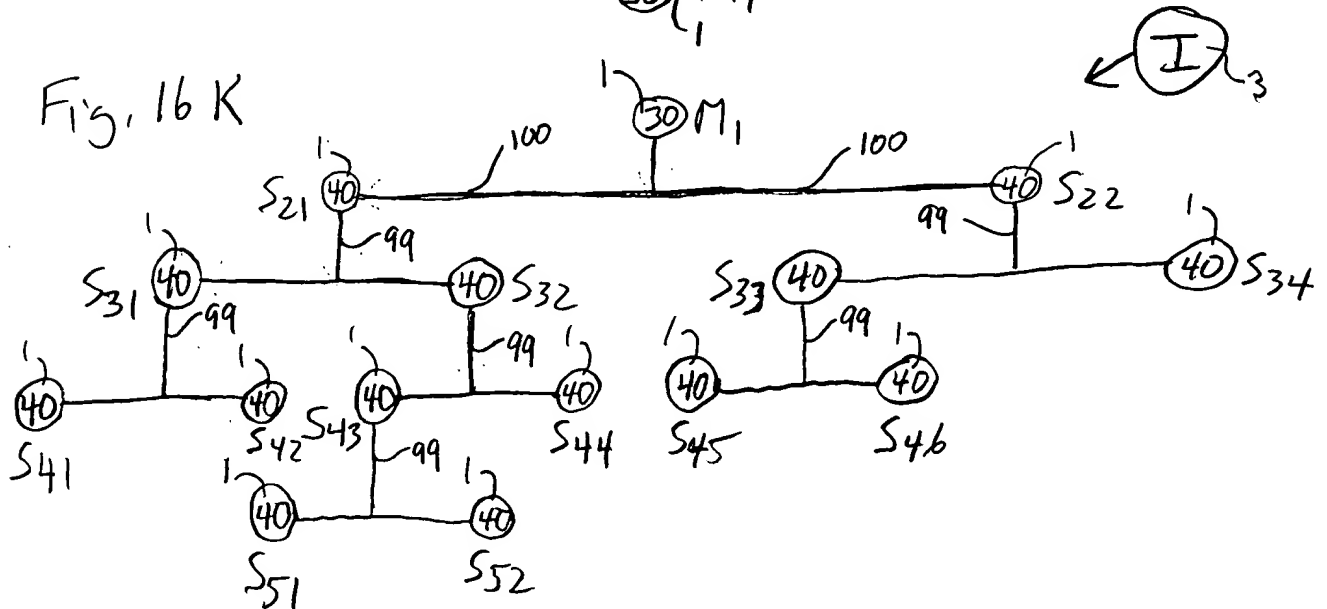


Fig. 16 K



2025 RELEASE UNDER E.O. 14176

11/17

Fig. 16L

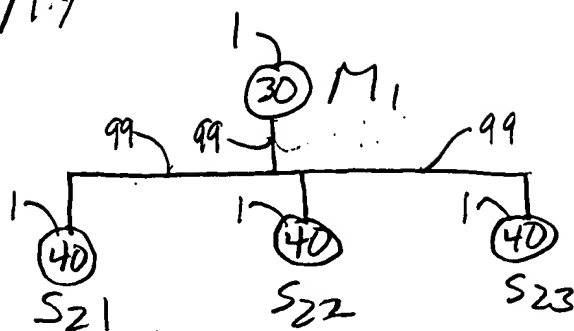


Fig. 16M

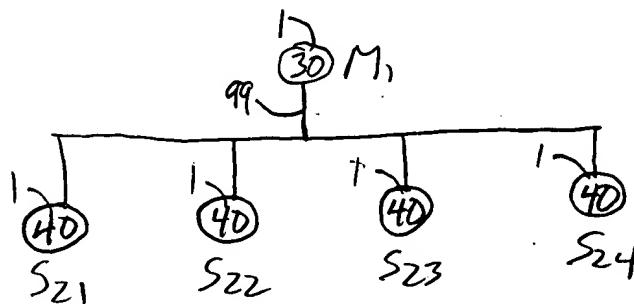


Fig. 16N

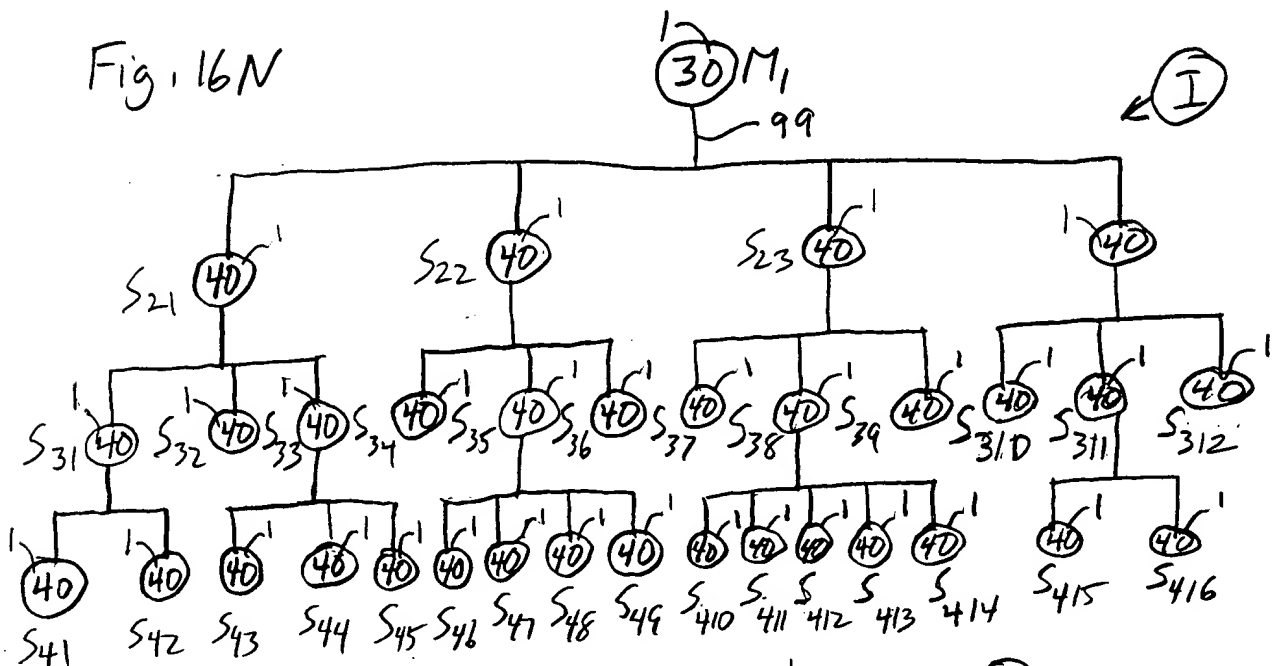


Fig. 16O

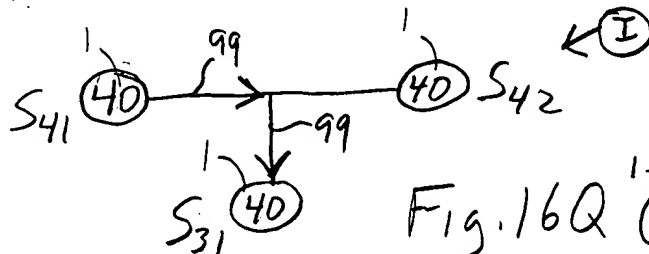


Fig. 16Q

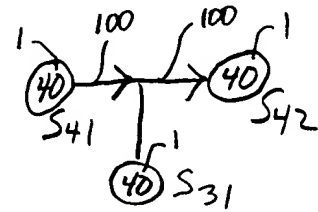
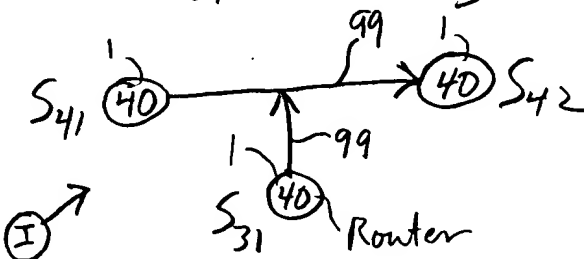


Fig. 16P



Figs. 16O-Q  
are sections  
of Fig 16 F  
Net (left upper)

12/17

like  
Fig 10A  
& 10B

Fig. 16X



Fig. 16Y

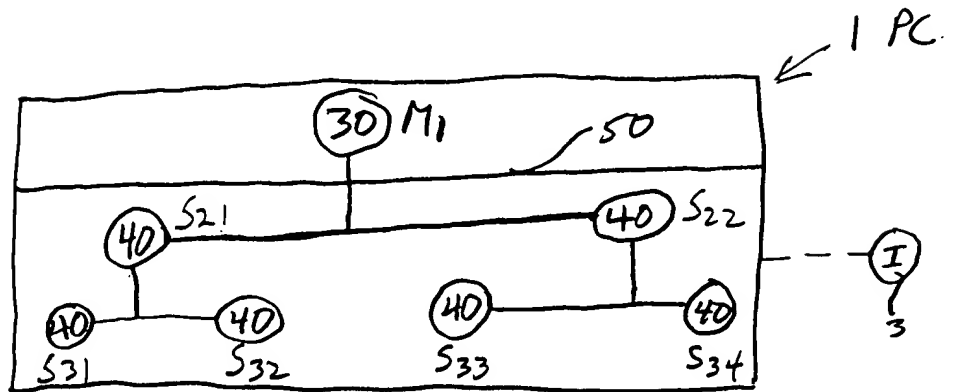


Fig. 16Z

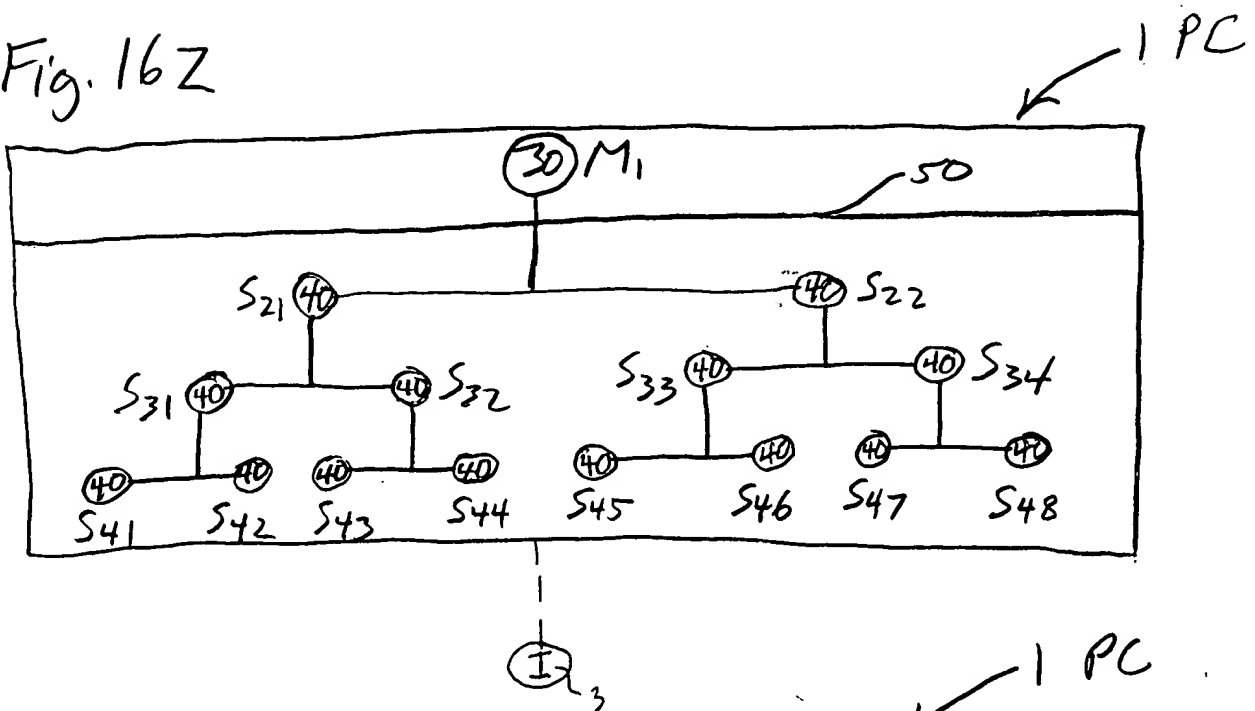
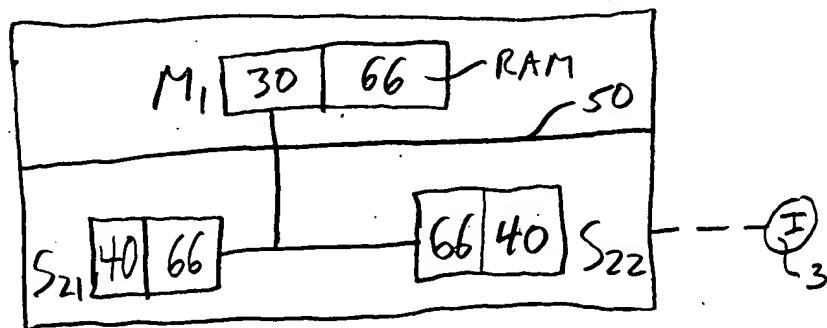
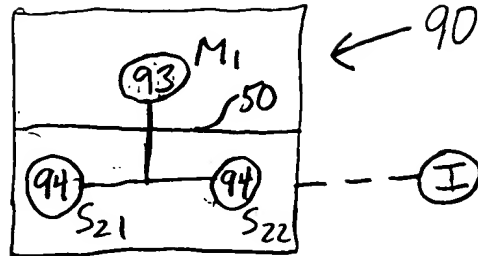


Fig. 16AA



13/17

Fig. 16R



Microchip

Like Fig. 10C:  
"Personal Computer  
on a chip"  
(Figs. 16R-16U)

Fig. 16S

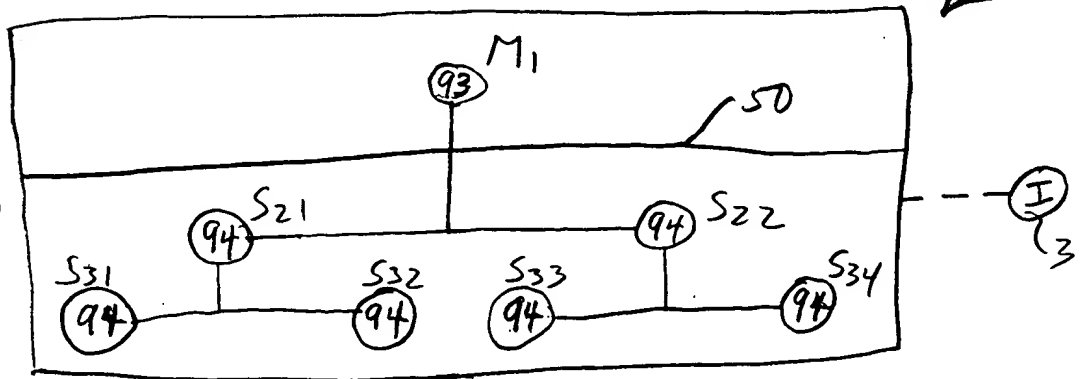


Fig. 16T

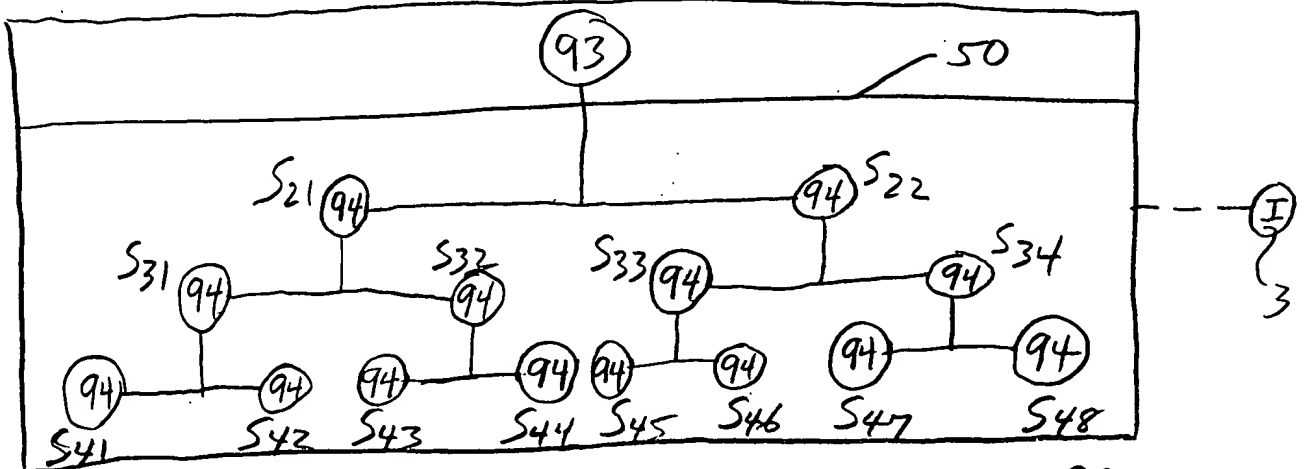
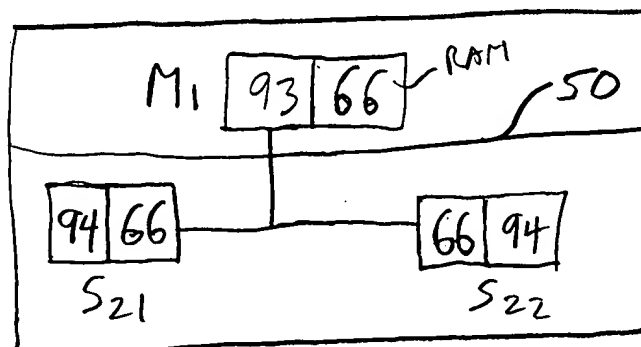


Fig. 16U



Microprocessors 90  
can be entire  
PCI on a single  
microchip

14/17

Fig. 16V

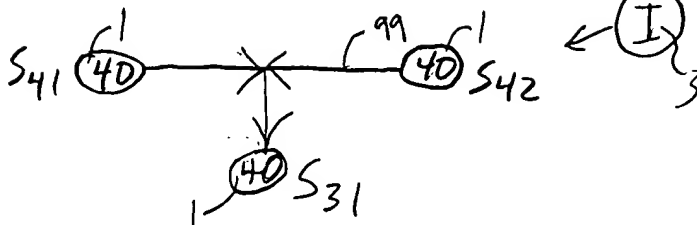


Fig. 16W-X  
follows Fig.  
16O-Q &  
are also sections  
of Fig. 16F net

Fig. 16W

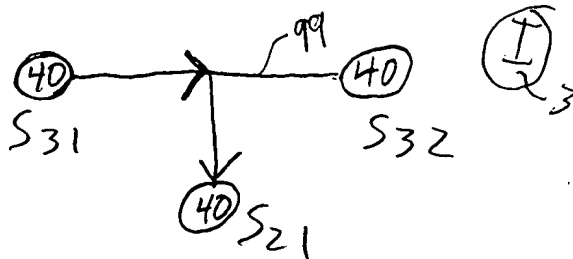


Fig. 17C

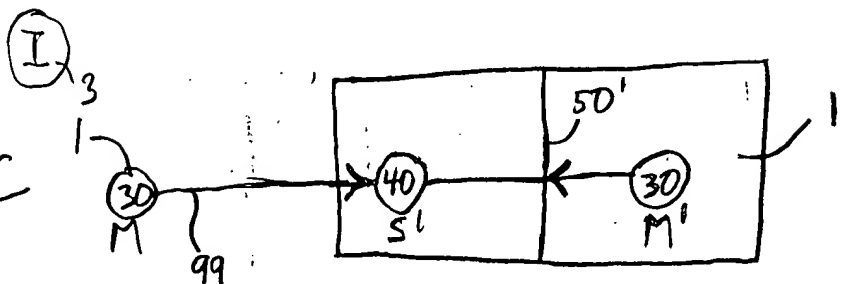


Fig. 17A

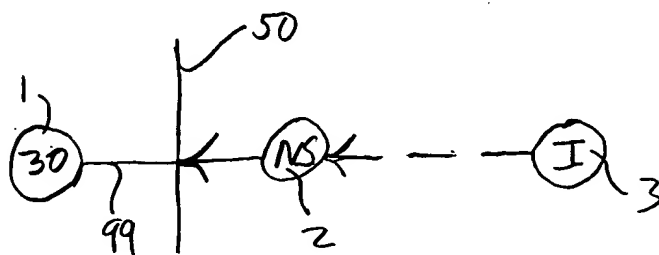


Fig. 17B

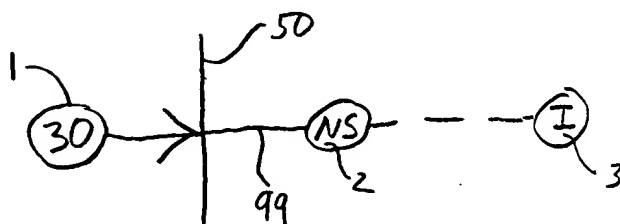
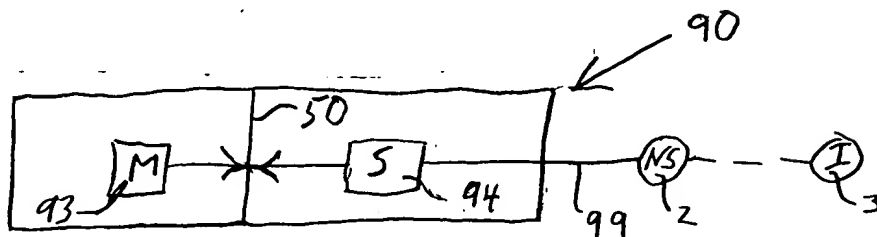
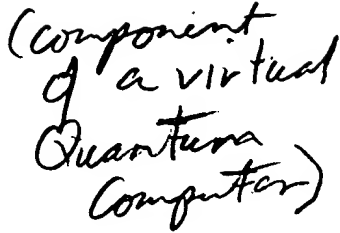


Fig. 17D

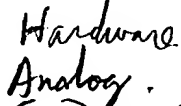


[illegible]

microprocessor



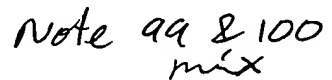
PC



Can also  
Simultaneously use  
of PC 1 for both  
digital & quantum  
computers.

and in Parker  
Fingers

Luke Fig. 13



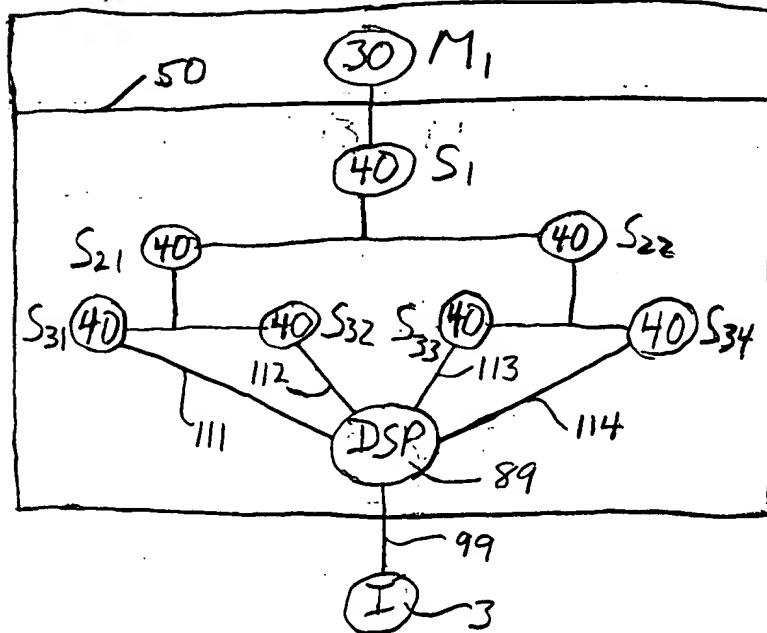
# of  $VQ$  can be scaled to any size Quantum Computer  $QC$





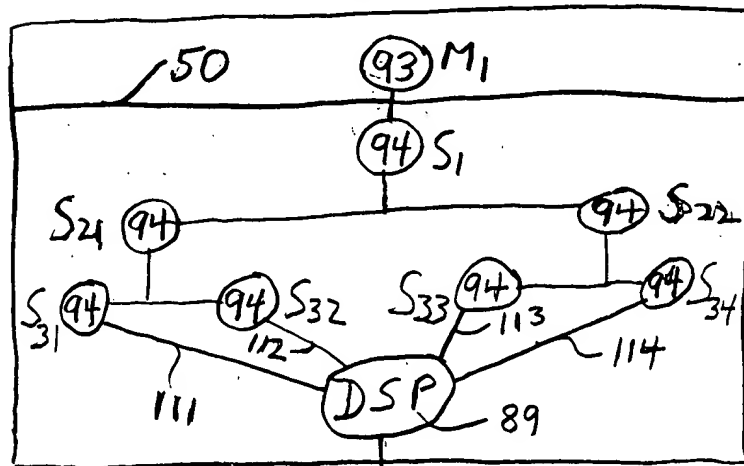
17/17

Fig. 20A



PC1  
←

Fig. 20B



PC  
90<sub>1</sub>  
←

